DTμL 9941 • DTμL 9951

MONOSTABLE MULTIVIBRATORS

DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS (TEMPERATURE RANGE: −55°C to 125°C)

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT

GENERAL DESCRIPTION — The DTμL 9941 and DTμL 9951 Monostable Multivibrators are monolithic silicon epitaxial integrated circuits for use with Fairchild Diode-Transistor Micrologic® Integrated Circuits or any other similar DTL logic elements. They provide complementary output pulses which are typically 150 ns wide. This pulse width is adjustable by the addition of external discrete passive components.

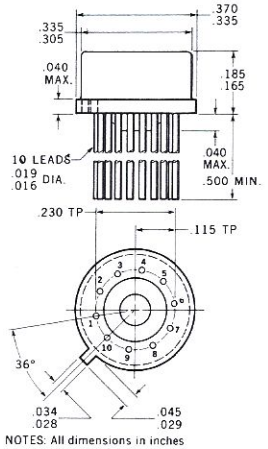
Both elements are compatible with the Fairchild DTμL Family over the full military temperature range of −55°C to +125°C and with a V_{CC} supply of 4.0 volts to 6.0 volts. They can also drive and be driven by Fairchild μL® Integrated Circuit .

The output pulse width is very stable as either V_{CC} or temperature (or both) is varied when an external timing resistor is used instead of the internal diffused resistor.

The DTμL 9941 has the same circuit as the DTμL 9951 with the addition of three series diodes from the extender pin (Pin 2) to ground. These diodes give the DTμL 9941 a DC threshold of about 1.5V which gives the circuit a greater than 2.0V noise immunity.

PHYSICAL DIMENSIONS

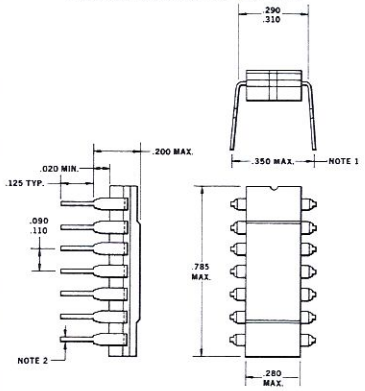
(In accordance with JEDEC TO−100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

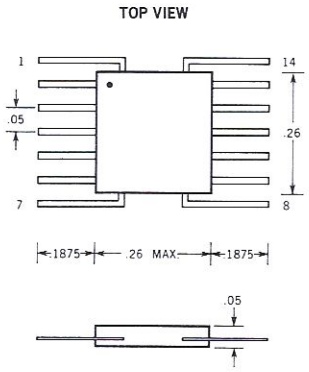
TYPICAL DUAL IN-LINE* PACKAGE

(In accordance with JEDEC TO−116)

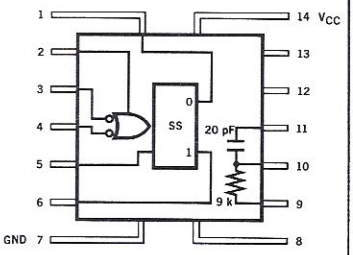


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

TYPICAL FLAT PACKAGE



CONNECTION DIAGRAM

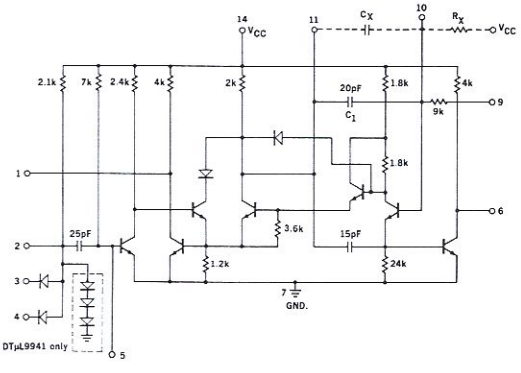


(Top View)

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Supply Voltage (V_{CC}) −55°C to +125°C, continuous:	+8.0 Volts
Supply Voltage (V_{CC}), pulsed, <1 second:	+12 Volts
Output Current, into outputs	50 mA
Current into Pin 10	5.0 mA
Input Forward Current	−10 mA
Input Reverse Current	1.0 mA
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

SCHEMATIC DIAGRAM



*Fairchild Patent Pending

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FAIRCHILD SEMICONDUCTOR
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TEST SEQUENCE

Test No.	CERPAK Pin no.: / TO-100 Pin no.:	FORCING FUNCTIONS 5	1 7	2 8	3 9	4 -	6 10	7 1	9 2	10 3	11 4	14 6	Note 1 Sense	Limits Min.	Max.
1				V_F				GND				V_{CCH}	I_2	$.5\ I_F$	
2					V_F	V_R		GND				V_{CCH}	I_3	$.5\ I_F$	$2\ I_F$
3	Note 2				V_R	V_F		GND				V_{CCH}	I_4	$.5\ I_F$	$2\ I_F$
4								GND			V_F	V_{CCH}	I_{11}	$.5\ I_F$	
5				GND	V_R			GND				V_{CCH}	I_3		I_R
6	Note 2			GND		V_R		GND				V_{CCH}	I_4		I_R
7			I_{OL}					GND		GND		V_{CCL}	V_1		V_{OL}
8		GND						GND	V_{CCL}			V_{CCL}	V_1		V_{OL}
9							I_{OL}	GND	V_{CCL}			V_{CCL}	V_6		V_{OL}
10			I_{OH}	GND				GND	V_{CCL}			V_{CCL}	V_1	V_{OH}	
11							I_{OH}	GND		GND		V_{CCL}	V_6	V_{OH}	
12								GND	V_{CCH}	GND		V_{CCH}	I_9	I_{9K}	I_{9K}
13					GND	GND		GND	V_{PD}			V_{PD}	$I_9 + I_{14}$		I_{PDL}
14					GND	GND		GND				V_{MAX}	I_{14}		I_{MAX}
15								GND	V_{CCH}			V_{CCH}	V_2	V_{2L}	V_{2H}
16	$t_{pd}-$ Pin 1	See Test Circuit, page 3													50 ns
17	$t_{pd}+$ Pin 6	See Test Circuit, page 3													50 ns
18	Pulse width Pin 1 (DTμL9951)	See Test Circuit, page 3												90	220 ns
19	Pulse width Pin 6 (DTμL9951)	See Test Circuit, page 3												70	160 ns
20	Pulse width Pin 1 (DTμL9941)													90	330 ns
21	Pulse width Pin 6 (DTμL9941)													70	270 ns

TABLE OF FORCING CONDITIONS

		−55°C	25°C	+125°C
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_{PD}	Volts		5.0	
V_{MAX}	Volts		8.0	
V_R	Volts		4.0	
V_F	Volts	0.0	0.0	0.0
I_{OL}	mA	15.0	15.0	14.0
I_{OH}	mA	−.18	−.18	−.18

TABLE OF TEST LIMITS

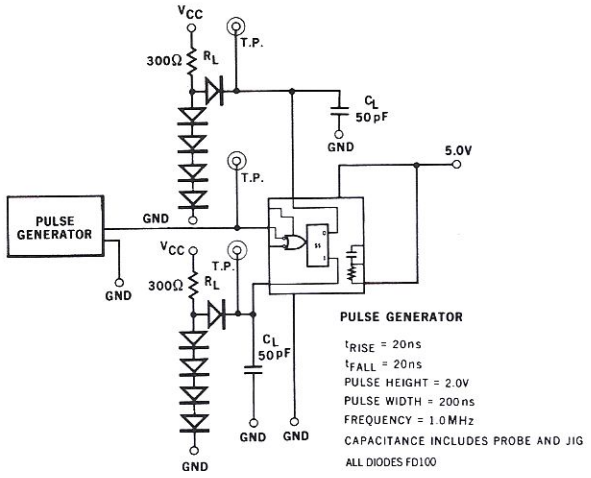
		−55°C Min.	−55°C Max.	25°C Min.	25°C Max.	+125°C Min.	+125°C Max.
$.51_F$	mA	−.80		−.80		−.75	
21_F	mA		−3.20		−3.20		−3.0
I_R	μA				5.0		10.0
V_{OL}	Volts		.40		.40		.45
V_{OH}	Volts	2.5		2.5		2.5	
I_{9K}	mA			.50	.75		
I_{PDL}	mA				9.0		
I_{MAX}	mA				22.0		
V_{2H}(9951)	Volts			5.0			
V_{2L}(9941)	Volts				2.5		

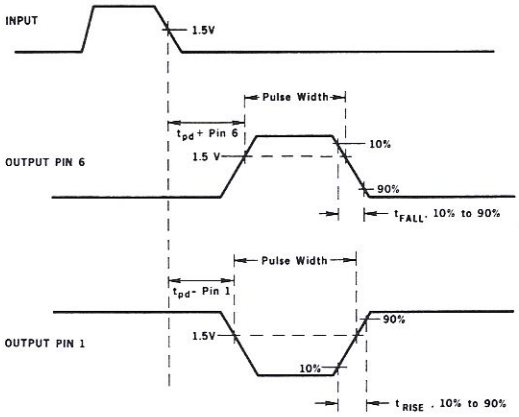
PURCHASING INFORMATION

To order the elements specify U3IXXX51X for Flat Package, U5FXXXX51X for TO-100 and U6AXXXX51X for Dual-In-Line*package (TO-116) where XXXX is the four-digit number denoting the specific element desired.

*Fairchild Patent Pending

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

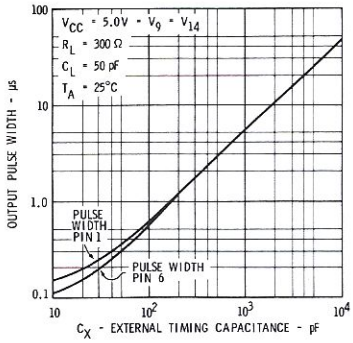




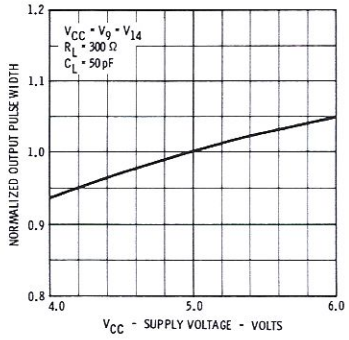
TIMING CHARACTERISTICS

(Test circuit above is used with appropriate modifications where necessary)

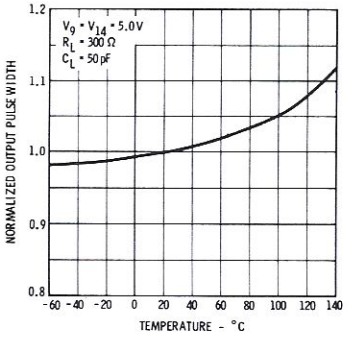
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X


V_{CC} = 5.0V = V_9 = V_{14}
R_L = 300Ω
C_L = 50pF
T_A = 25°C
PULSE WIDTH PIN 1
PULSE WIDTH PIN 6
OUTPUT PULSE WIDTH - μs
C_X - EXTERNAL TIMING CAPACITANCE - pF

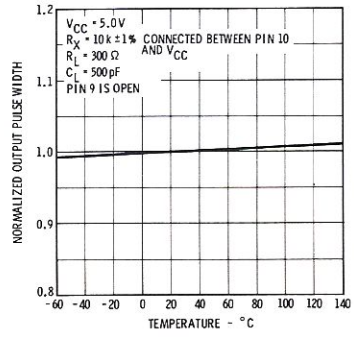
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



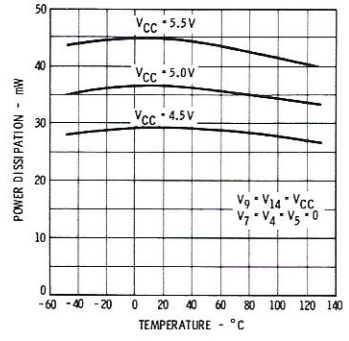
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



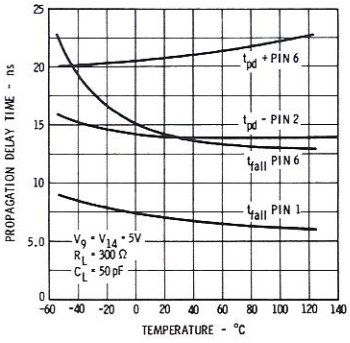
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X


V_{CC} = 5.0V
R_X = 10k ±1% CONNECTED BETWEEN PIN 10 AND V_{CC}
R_L = 300Ω
C_L = 500pF
PIN 9 IS OPEN
NORMALIZED OUTPUT PULSE WIDTH
TEMPERATURE - °C

TYPICAL POWER DISSIPATION VERSUS TEMPERATURE



SWITCHING TIMES VERSUS TEMPERATURE



FAIRCHILD DTμL INTEGRATED CIRCUITS 9941 • 9951

RULES FOR USE OF DTμL 9941 AND DTμL 9951

1. With Pin 9 connected to V_{CC} and no external capacitor (C_x), the output pulse width is approximately 150 ns.

2. With Pin 9 connected to V_{CC} and an external capacitor (C_x) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_x + 20)$ with C_x in pF and T in ns.

3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_x) of 9 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5R_x\ (C_x + 20)$ with R_x in kΩ, C_x in pF and T in ns.

4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2 kΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.

5. The maximum input fall time to trigger: 25 ns for a 1.0 volt swing; 50 ns for a 2.0 volt swing; 100 ns for a 4.0 volt swing.

6. The minimum pulse width at output Pin 1 is approximately 100 ns. This pulse width may be decreased to 50 ns by connecting a 10 kΩ resistor between Pin 5 and V_{CC}.

USE OF DTμL 9941 AND DTμL 9951 WITH MICROLOGIC® INTEGRATED CIRCUITS

The DTμL 9951 may be operated from a V_{CC} supply of 4.0 to 6.6 volts. Operation is essentially independent of output resistive and capacitive loading. The input triggering action is initiated by a negative-going input with an amplitude change of 1.0 volt or more. The DTμL 9941 requires the input to go at least one volt below its 1.5 V threshold.

RTμL and Low Power RTμL outputs can drive the DTμL 9941 and DTμL 9951 inputs, provided the output swing is greater than 1.0 volt. Either of the outputs of the DTμL 9941 and DTμL 9951 can drive RTμL and Low Power RTμL inputs. Fan-out from the DTμL 9941 and DTμL 9951 is 4 RTμL unit loads and 1 Low Power RTμL unit load, for the DTμL 9941 and DTμL 9951 $V_{CC} \geq 4.0$ volts. Use of a resistor of 500Ω to 1kΩ from the DTμL 9941 and DTμL 9951 output to V_{CC} will increase fan-out into Low Power RTμL, or RTμL.

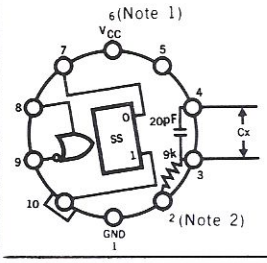
INPUT-OUTPUT LOAD FACTORS TO DTμL FAMILY

Each DTμL 9941 and DTμL 9951 input should be rated at 2 loads.

Each DTμL 9941 and DTμL 9951 output may drive 10 DTμL loads.

For input-output load factors of other DTμL elements, please refer to the DTμL Composite Data Sheet and to the individual DTμL element specifications.

TO-100 TYPE CONNECTION DIAGRAM (Top View)



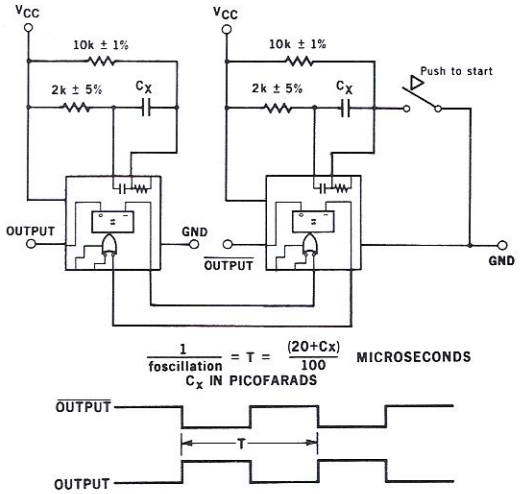
NOTES:

(1) The V_{CC} supply pin is not the tabbed pin on the DTμL 9951.

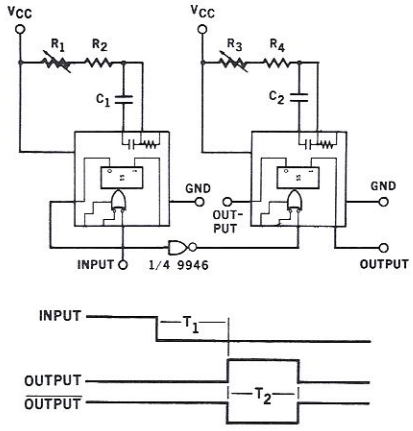
(2) Connect to V_{CC} when R external is not used.

All data in this specification refers to 14-pin Cerpak pin numbers except this outline and the 10-pin reference numbers in the test sequence on Page 2.

STABLE MULTIVIBRATOR



VARIABLE DELAY PULSE GENERATION



Explanation

The input 9951 determines T_1, the time before the initiation of the output pulse. The second or output 9951 determines T_2, the output pulse width.

With $R_2 = 10$ kΩ and R_1 a 5 kΩ potentiometer, T_1 is variable over a range of 2 to 3 and is given by $T_1 \approx 0.5\ (R_1 + R_2)\ (C_1 + 20$ pF).

Similarly, with $R_4 = 10$ kΩ and R_3 a 5 kΩ potentiometer, T_2 is $\approx 0.5\ (R_3 + R_4)\ (C_2 + 20$ pF) and T_2 can be controlled by the potentiometer over a range of 2 to 3 since 10 kΩ $\leq (R_3 + R_4) \leq$ 15 kΩ.

A much greater range in T_1 and T_2 is available by varying C_1 and C_2.

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